 from ACS News-letter #182

A 1200 BAUD KC STD. INTERFACE FOR THE SWTP 6800

EVER SINCE I GOT MY SYSTEM UP AND RUNNING, A 1200 BAUD CASSETTE MODEM HAS BEEN LIKE MT. EVEREST FOR ME - - I WANTED (TO CLIMB) IT - BECAUSE IT WAS THERE! OF COURSE, IT DID'NT BOTHER ME TOO MUCH AT FIRST. AT THAT POINT, ANY SORT OF CASSETTE INTERFACE WAS GOOD ENOUGH! SO I THREW TOGETHER A CRUDE 300 BAUD "MODEM" USING THE POPULAR KANSAS CITY STANDARD FREQUENCIES, 2400 HZ FOR A 1 AND 1200 HZ FOR A 0.

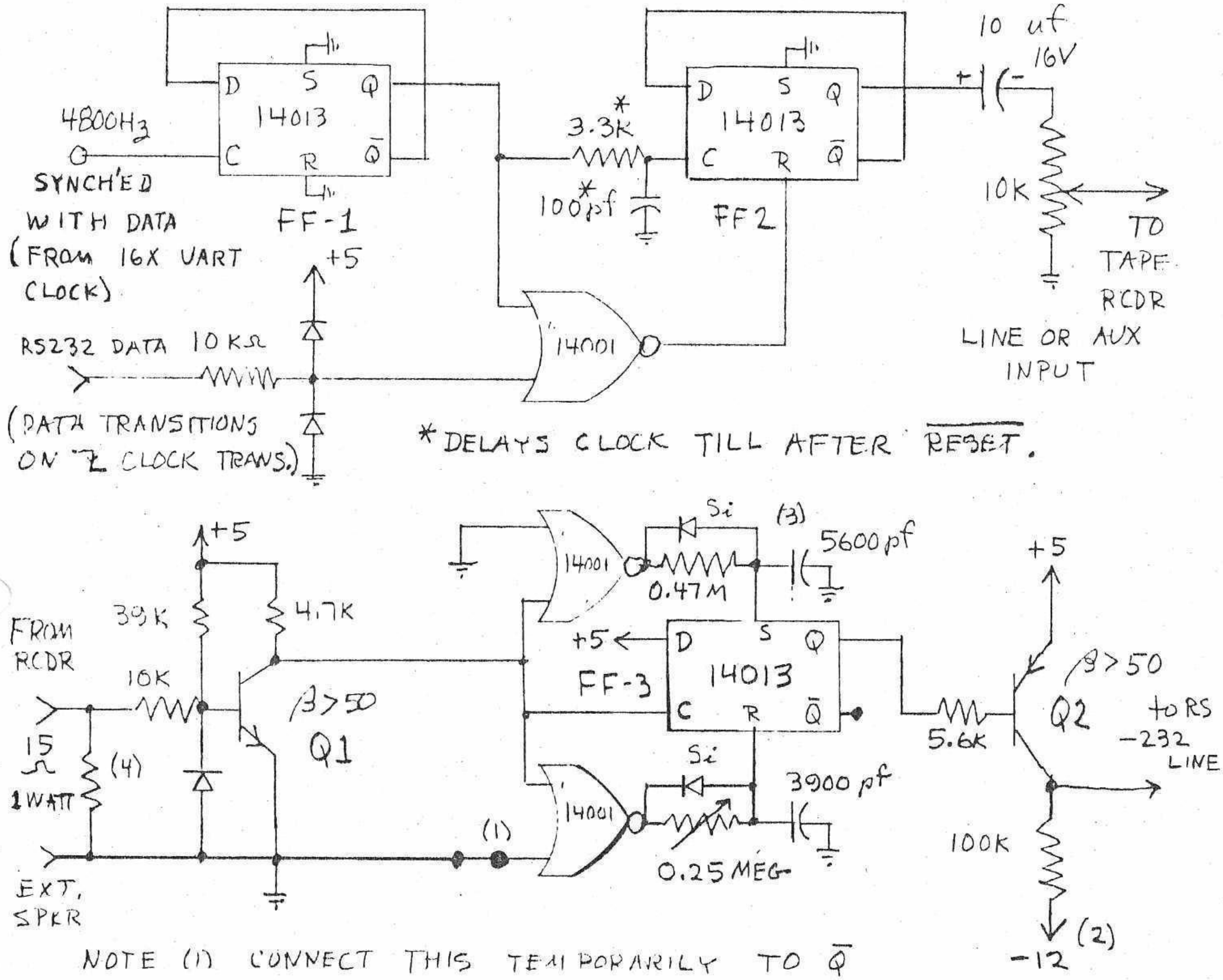
THE CIRCUIT, SHOWN IN FIGURE 1, USES A QUAD NOR GATE AND A PAIR OF DUAL TYPE D FLIPFLOPS. THE 4800 CLOCK SIGNAL FROM THE COMPUTER IS FIRST DIVIDED BY 2 TO OBTAIN 2400 HZ FOR THE 1'S. DURING LOGIC 0'S (RS232 LINE HIGH) THE RESET OF FF-2 IS HELD LOW, SO IT FURTHER DIVIDES THE FREQUENCY BY 2 AGAIN TO OBTAIN 1200 HZ. DURING LOGIC 1'S (RS232 LINE LOW) THE NOR GATE RESETS FF-2 ON THE NEGATIVE TRANSITIONS OF ITS CLOCK INPUT, SO FF-2'S OUTPUT IS 2400 HZ. THE SQUARE WAVES CAN BE FED DIRECTLY TO THE TAPE RECORDER THROUGH A LEVEL ADJUSTING POTENTIOMETER.

ON PLAYBACK, EXCESSIVE DIFFERENTIATION AND DISTORTION OF THE SQUAREWAVES IS AVOIDED BY LOADING THE TAPE RECORDER OUTPUT WITH A RESISTOR 2 TO 3 X'S THE NORMAL LOAD. AN 8 OHM SPEAKER CAN BE REPLACED BY ABOUT 15 TO 22 OHMS, WHILE A 30 OHM "EAR" OUTPUT COULD BE LOADED BY 68 TO 100 OHMS. THIS RESISTIVE LOAD SHUNTS THE INDUCTANCE OF THE OUTPUT TRANSFORMER OF THE TAPE RECORDER, PREVENTING ITS RISING IMPEDANCE WITH FREQUENCY FROM DISTORTING THE SQUARE WAVES. Q1 SQUARES UP THE TAPE RECORDER OUTPUT. IT IS DC BIASED SO THAT IN THE ABSENCE OF SIGNAL ITS COLLECTOR GOES LOW, WHICH SETS FF-3, CUTTING OFF Q-2 AND "RELEASING" THE RS232 LINE. WITH TAPE SIGNAL PRESENT, THE DETECTOR CIRCUIT ATACHED TO THE SET TERMINAL OF FF-3 REMOVES THE SET INPUT. FOR 2400 HZ, THE RESET INPUT REMAINS BELOW THE TRIGGER LEVEL AND THE CLOCK INPUT PULLS Q OF FF-3 HIGH, CUTTING OFF Q-2, AND ALLOWING THE LINE TO GO LOW. WHEN THE 1200 HZ SIGNAL IS PRESENT, THE RESET EXCEEDS THE TRIGGER LEVEL BEFORE THE CLOCK EDGE AND INHIBITS IT - THUS Q REMAINS LOW, WHICH TURNS ON Q-2 AND PULLS THE LINE HIGH.

THIS SIMPLE CIRCUIT SUFFICED FOR QUITE A WHILE, AND JOE DUBNER, OF ACS, AND I WERE ABLE TO EXCHANGE TAPES, IN SPITE OF SLIGHT DIFFERENCES IN OUR CLOCK FREQUENCIES AND TAPE RECORDER SPEEDS.

THEN I BEGAN TO CONSIDER MAKING TAPES FOR SALE TO OTHERS, AND REALIZED THAT THEY WERE GOING TO HAVE TO BE SUITABLE FOR PLAYBACK ON A VARIETY OF RECORDERS, SOME PROBABLY NOT OF THE QUALITY OF MINE. I USED DON LANCASTER'S CLASSIC ARTICLE IN THE MARCH '76 BYTE MAGAZINE AS MY "BIBLE", AND DECIDED THAT SINEWAVE RECORDING WAS THE ONLY RELIABLE TYPE. I BUILT A VARIATION OF DON'S "BIT BOFFER" AND STARTED USING IT. HOWEVER, AFTER TRY-

FIG 1 SIMPLE KANSAS CITY STANDARD CASSETTE INTERFACE FOR 300 BAUD OPERATION



NOTE (1) CONNECT THIS TEMPORARILY TO Q̄ AND PLAY BACK ALTERNATING 1'S AND 0'S TO ADJUST 0.25MEG CONTROL FOR OPTIMUM SEPARATION OF 1'S AND 0'S, USING 'SCOPE ON OUTPUT.

NOTE (2) THIS CAN BE RETURNED TO GROUND IF A PARALLEL PERIPHERAL IS ALREADY PULLING LINE TO -12V.

NOTE (3) PURPOSE: TO CUT OFF OUTPUT TRANSISTOR WHEN NO TONE PRESENT

NOTE (4) CHOOSE TO SUIT RECORDER OUTPUT

R YOST
265-8047

ING A CIRCUIT LIKE HIS FOR RECOVERING THE CLOCK, I BECAME DISENCHANTED WITH ITS TRADEOFF BETWEEN ADEQUATELY WIDE CLOCK PULSES AND SPEED TOLERANCE, AND WITH ITS SENSITIVITY TO RANDOM ERRORS. I WANTED TO USE DON'S SINEWAVE SYNTHESIZER, BUT DIDN'T WANT TO INSTALL SWITCHES IN MY COMPUTER TO SWITCH TO THE 19.2 KHZ CLOCK FOR IT, SO I DECIDED TO INCLUDE A PHASE LOCKED LOOP CLOCK GENERATOR RUNNING AT 19.2 KHZ, WITH TWO DIVIDERS TO OBTAIN 4800 HZ TO PHASE COMPARE WITH A 4800 HZ SIGNAL DERIVED FROM THE TAPE RECORDER'S ZERO CROSSINGS.

IT WAS THEN THAT SOME OF THE PECULIARITIES OF THE DATA STREAM GENERATED BY MIKBUG'S SOFTWARE UART CAME TO LIGHT. BECAUSE A DATA WORD (A 0 START PULSE, 8 DATA BITS, AND A 1 STOP PULSE) COULD START ON ANY ONE OF THE 4800 HZ CLOCK PULSES, THE 2400 AND 1200 HZ SIGNALS DERIVED FROM THE TAPE WERE NOT SYNCHRONOUS WITH THE DATA, THUS AS FREQUENCIES, THEY WEREN'T VERY STABLE. LANCASTER PROVIDED A SYNCH CONNECTION FROM HIS SINE SYSTHESIZER TO THE DIVIDER FF'S, WHICH GENERATED EXTRA CLOCK PULSES; THIS MADE A CLOCK RECOVERED FROM THE RECORDED DATA EVEN FURTHER FROM A STABLE 4800 HZ CLOCK SUITABLE FOR THE MIKBUG SOFTWARE UART.

NONETHELESS, AFTER CLEANING UP THIS CIRCUIT, I WAS ABLE TO GET IT WORKING WELL AT 300 AND 600 BAUD - BUT NEVER AT 1200 BAUD! EVEN AT 600, I FOUND THAT IT WAS BEST NOT TO USE LANCASTER'S SYNCH CONNECTION.

RECENTLY, I DECIDED TO TRY AGAIN TO SCALE THE 1200 BAUD "PEAK". I DECIDED TO RECLOCK THE DATA COMING OUT OF MIKBUG, USING FOR A CLOCK ONE OF THE SQUARE WAVE OUTPUTS OF THE SINEWAVE SYNTHESIZER. THUS, REGARDLESS OF WHAT CYCLE OF THE 4800 HZ CLOCK A WORD STARTED ON, RECLOCKING IT WITH A D FLIPFLOP WOULD DELAY IT ENOUGH TO KEEP THE BIT EDGES SYNCHRONOUS WITH THE SINEWAVES. IN OTHER WORDS, I COULD FORCE THE DATA TO ALWAYS CHANGE AT, SAY, THE SINEWAVE ZERO CROSSINGS, OR AT OTHER CONTROLLED PHASES.

TO MY SURPRISE, THIS TOO FAILED TO WORK AT 1200 BAUD. I THOUGHT THE TROUBLE WAS IN MY DATA RECOVERY CIRCUITS, BUT WHEN DUBNER BROUGHT OVER A TAPE HE'D RECORDED AT 1200 BAUD AND I WAS ABLE TO SUCCESSFULLY LOAD IT INTO THE SWTP 6800 USING THE MIKBUG LOAD COMMAND, I BEGAN TO LOOK AT MIKBUG'S OUTPUT MORE CLOSELY.

DUBNER HAD USED AN ACIA RATHER THAN THE MIKBUG SOFTWARE UART. THAT CLUE LED TO DISCOVERY OF THE PROBLEM. AT 1200 BAUD, MIKBUG'S START PULSES WERE SOMETIMES 17 CLOCK PERIODS LONG, INSTEAD OF 16. APPARENTLY, IF THE BIT LENGTH TIMER IS RESET JUST AFTER A CLOCKING EDGE, THE JUST-UNDER-1-CLOCK-PULSE DELAY TILL THE NEXT PULSE, COMBINED WITH THE SOFTWARE DELAYS, RESULT IN THE 17 CLOCKPERIOD START BIT. MY D FLIP-FLOP WAS GENERATING ANOTHER 0 FOLLOWING

THE START PULSE (ALWAYS A Ø) EVEN WHEN THE FIRST DATA BIT WAS A 1.

THIS CHARACTERISTIC SHOULD NOT BE THOUGHT OF AS A "BUG" IN MIKBUG. WILES & FELIX (FOOTNOTE 1) SHOW MIKBUG CONTROLLING A

FOOTNOTE 1: WILES AND FELIX, "ENGINEERING NOTE 1ØØ, MCM683ØL7 MIKBUG/MINIBUG ROM", MOTOROLA SEMICONDUCTOR PRODUCTS, INC

PROGRAMMABLE COUNTER DIVIDING AN INTERNALLY GENERATED CLOCK BY 16,384 AND 32,768, RATHER THAN BY 8 AND 16, AS IN THE SWTP68ØØ SERIAL CONTROL INTERFACE. ON THE OTHER HAND, THE MATTER OF 17 CLOCK PULSES FOR THE START BIT IS OF NO CONSEQUENCE TO ANY WELL DESIGNED UART. ONE APPROACH TO A FIX WOULD HAVE BEEN TO INCLUDE A UART IN MY CASETTE INTERFACE TO RECLOCK THE DATA. BUT THAT WOULD HAVE MADE IT MUCH MORE COMPLEX.

AFTER SOME THOUGHT, I CONCLUDED THAT THE ONLY OTHER WAY AROUND THIS WAS TO FORCE MIKBUG TO FIRST OUTPUT A 1, TO GET THE TIMER STARTED PROPERLY. MY MODEM WOULD IGNORE THE 1, AS IT ASSUMES THE TIME BETWEEN WORDS IS ANY RANDOM NUMBER OF 48ØØ HZ CLOCK PERIODS, AND THE 17 PULSE LONG 1 BIT WOULD BE INDISTIGUISHABLE FROM THE INTERWORD MARK (1) CONDITION ON THE RS232 LINE.

I WROTE A SHORT PROGRAM, BASED ON MIKBUG'S PROGRAMMING, AND MAKING MAXIMUM USE OF MIKBUG SUBROUTINES. IT IS SHOWN IN LISTING NO 1. IT CAN BE LOADED INTO RAM IN ANY CONVENIENT LOCATION. PROGRAMS FOR WHICH 12ØØ BAUD OUTPUT IS DESIRED MUST JUMP TO THIS SUBROUTINE RATHER THAN TO MIKBUG'S "OUTEEE". I HAVE WRITTEN IT INTO MY 8 K BASIC, AND INTO THE EDITOR/ASSEMBLER I'M USING. I'VE ALSO WRITTEN AN OPERATING SYSTEM, OF SORTS, AUGMENTING MIKBUG'S FUNCTIONS, AND THIS 12ØØ BAUD PROGRAM IS INCLUDED THEREIN.

Editors note:

This article will be completed in the April issue of ACS I/O Port.

I wish to thank Russ Yost for this the first article in this newsletter and to try and incourage fellow members to try their luck at writting similar articles. Thanks again.

The Editor

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LOC  B1 B2 B3

357C             >********************
357C             >*                  *
357C             >*   SERIAL OUTPUT  *
357C             >*   SUBROUTINE FOR *
357C             >*   1200 BAUD      *
357C             >*                  *
357C             >*  R YOST, NOV '77 *
357C             >*                  *
357C             >********************
357C             >
E1A5             >SAV    EQU   $E1A5  MIKBUG SR. USED IN MIKBUG OUTEEE SR.
E1F3             >DE     EQU   $E1F3  MIKBUG TIMER SR.
E1EF             >DEL    EQU   $E1EF     DITTO
E1DA             >RET    EQU   $E1DA  ENTRY POINT INTO MIKBUG OUTEEE SR.
357C             >
2000             >       ORG   $2000  ARBITRARY ORIGIN. MAY BE SET ANYWHERE.
2000 37          >OUTH   PSHB         SAVE B REGISTER
2001 BD E1 A5    >       JSR   SAV    SAVE X REG. & SET IT TO PIA ADDR.
2004 C6 0A       >       LDAB  #$A    SET UP COUNTER FOR 10 TOTAL BITS
2006 BD E1 F3    >       JSR   DE     START TIMER AND DELAY FOR 1 BIT, WHILE
2009 BD E1 EF    >       JSR   DEL     OUTPUTTING A "WARMUP" 1.
200C 6A 00       >       DEC   0,X    SET START BIT = 0.
200E 7E E1 DA    >       JMP   RET    JUMP INTO MIKBUG OUTEEE SR. FOR  REST OF
2011             >*                    DATA.
2011             >       END

<<< UNRESOLVED ITEMS >>>


<<< SYMBOLS >>>

DE    E1F3  DEL  E1EF  OUTH 2000  RET  E1DA  SAV  E1A5
C
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MINUTES OF THE APRIL 78 MEETING OF THE ACS BOARD OF DIRECTORS

By Jim Sheafor, Secretary

The regular monthly meeting of the Board of Directors of the Arizona Computer Society was held at the General Electric Building on April 19 at 7:30 PM. Present were Harry Stanton, President; Otto Weeden, Vise-President; Jim Sheafor, Secretary; Bob Thiel, Editor; Ray Moore and Russell Yost, Directors.

Under new business the following Action Items were undertaken:

1. A discussion of plans for holding a Swap Meet in the near future with assignments to board members to investigate possibilities.
2. A discussion of plans to hold a Computer Fair to be sponsored by ACS inconjunction with other computer clubs and user-groups in the area. METROCENTER was suggested as a potential site.

Under old business the following Action Items were undertaken:

1. Newsletter: The second issue of the newsletter will complete Russ Yost's cassette interface article and other inputs to be supplied by board members. No new inputs have been received.
2. Data Base forms will be available for new members at the next general meeting.

The meeting was adjourned at 9:00 Pm by the general consent of all directors present.

and now the conclusion of Russ Yost's article

A 1200 BAUD KC STD. INTERFACE FOR THE SWTP 6800

NOW, WHAT HARDWARE IS NEEDED TO INTERFACE WITH THIS 1200 BAUD OUTPUT SOFTWARE?
FIGURE 2 IS A LOGIC DIAGRAM AND SCHEMATIC DIAGRAM OF MY MODEM. IT IS DESIGNED TO INTERFACE TO A SWTP CT1024 TERMINAL, BUT CAN READILY BE ADAPTED TO OTHER 6800 SYSTEMS. IT IS TIED IN PARALLEL WITH THE CT1024 ON THE RS232 LINES FROM AND TO THE COMPUTER. THE MODEM COMMUNICATES WITH THE COMPUTER OR THE TERMINAL, ACCORDING TO SWITCH S2'S POSITION. TERMINAL "ROC" IS THE COMPUTER RS232 OUTPUT LINE; "RIC" DENOTES THE COMPUTER INPUT RS232 LINE. "COC" IS THE 4800 HZ CLOCK OUTPUT OF THE COMPUTER. THE COMPUTER BAUD RATE SELECTOR IS LEFT AT 300 AND DOES NOT HAVE TO BE CHANGED FOR THE OTHER RATES. "CIC" IS THE CLOCK SIGNAL AT 4800,9600,OR 19200 HZ RETURNED TO THE TERMINAL AND COMPUTER FROM THE MODEM. THIS CLOCK IS SUPPLIED CONTINUALLY, WHETHER THE MODEM IS IN USE OR NOT. POWER IS SUPPLIED AT ALL TIMES TO THE MODEM FROM THE CT1024 +5 AND -12 SUPPLIES.

IF THE TAPE RECORDER OUTPUT SIGNAL IS ABSENT, THE COC SIGNAL IS SELECTED FOR THE PHASE LOCKED LOOP REFERENCE, BY NAND GATE IC-4-C.

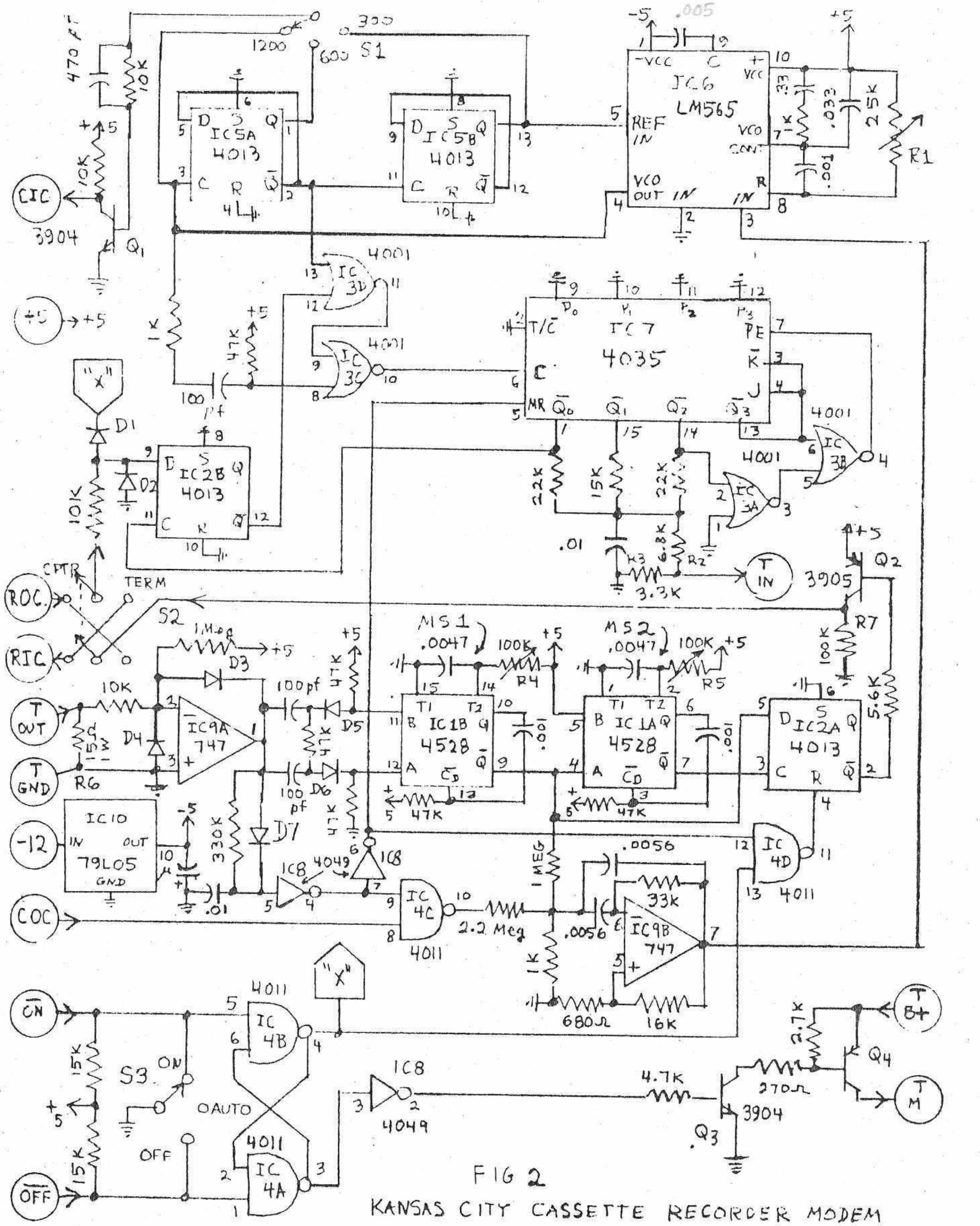

FIG 2

KANSAS CITY CASSETTE RECORDER MODEM
300, 600, 1200 BAUD, FOR SWTP 6800/CT1024
R YOST 771009

CONSIDER THE MODULATION FUNCTION. THE DATA IS FIRST LIMITED BY DIODES D1 AND D2. D1 IS GROUNDED IF THE TAPE RECORDER MOTOR IS TURNED OFF TO SUPPRESS DATA RECORDING IF THE MOTOR IS OFF, EVEN IF IT IS STILL COASTING AT SPEED. THE SWTP CT-1024 CRT TERMINAL USES CERTAIN CONTROL CHARACTERS TO TURN THE TAPE RECORDER MOTOR OFF AND ON. THESE DON'T OCCUR IN ASCII, BUT IN RECORDING IN "BINARY" FORMAT, THEY DO. TO GET AROUND THIS DIFFICULTY, BINARY RECORDING PROGRAMS MUST DETECT SUCH CHARACTERS AND SEND THE TAPE RECORDER A "TURN-ON" CHARACTER TO KEEP THE RECORDER MOTOR FROM STOPPING. THESE INSERTED CHARACTERS ARE NOT ADDED INTO THE CHECKSUM, AND SHOULD NOT BE RECORDED ON THE TAPE - THUS THE SUPPRESSION FUNCTION CONTROLLED BY THE MOTOR COMMANDS.

AT 1200 BAUD, WITH CERTAIN CRT INTERFACES, A DELAY MAY BE NEEDED BEFORE SENDING THE TURN-ON CHARACTER. WITH THE CT-1024, WRITING A CHARACTER ON THE LOWER PART OF A "PAGE" TAKES ENOUGH TIME THAT THE TURN-OFF CHARACTER MAY BE HELD IN THE UART'S OUTPUT REGISTER FOR SEVERAL BIT TIMES. SINCE THE DATA TO THE CASSETTE INTERFACE IS NOT PASSING THROUGH THE UART, THE TURN-BACK-ON CHARACTER COULD ARRIVE BEFORE THE TURN-OFF COMMAND IS RECEIVED FROM THE UART, SO THAT A PORTION OF THE TURN-BACK-ON CHARACTER WOULD BE RECORDED ON THE TAPE.

THE DELAY IS INSERTED BY A SIMPLE MODIFICATION TO THE SOFTWARE BINARY RECORDING PROGRAM. A DUAL NESTED SOFTWARE COUNTING LOOP CAN SUPPLY THE NEEDED DELAY. THIS HAS A NEGLIGIBLE EFFECT ON OVERALL SPEED, AS THE DELAY IS INVOKED ONLY AFTER THE RELATIVELY RARE TURN-OFF CHARACTERS.

LISTING 2 SHOWS THE MODIFICATIONS NEEDED TO SWTP'S "BIPUNCH" PROGRAM, AS DESCRIBED ON PG 13 OF THEIR SECOND NEWSLETTER, DATED OCT, 1976.

IC-2B PERFORMS THE RECLOCKING OF THE DATA. AS MENTIONED BY LANCASTER, I FOUND THAT CLOCKING IT SO THE DATA CHANGES 45 DEGREES BEFORE THE SINEWAVE GOES THROUGH ZERO MAINTAINS THE ZERO CROSSING SPACING RATIO FOR 0'S AND 1'S CLOSEST TO THE OPTIMUM OF 2:1. THIS LEAD TIME COULD BE A FUNCTION OF INDIVIDUAL TAPE RECORDER CHARACTERISTICS, SO EXPERIMENTATION MAY BE IN ORDER TO CHOOSE THE OPTIMUM OUTPUT PIN OF IC-7.

[ ]

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LOC  B1 B2 B3

1EC3             >*******************
1EC3             >*                 *
1EC3             >* MOD'N TO SWTP   *
1EC3             >*  BIPUNCH, PG 13 *
1EC3             >* NEWSLETTER #2   *
1EC3             >*   OCT. 1976     *
1EC3             >* FOR 12ØØ BAUD   *
1EC3             >*  WITH 64 CHAR   *
1EC3             >* VERSION OF      *
1EC3             >*  CT 1Ø24 CRT    *
1EC3             >* INTERFACE       *
1EC3             >*                 *
1EC3             >*  R YOST         *
1EC3             >*     OCT 1977    *
1EC3             >*                 *
1EC3             >*******************
1EC3             >
1E93             >PNON   EQU    $1E93   A SR. IN SWTP "BIPNCH"; TURNS ON RECORDER
1EC3             >*                       BY SENDING A $12 TO CT1Ø24, WHERE IT IS
1EC3             >*                       DECODED AS A "TURN ON RECORDER" COMMAND
1EC3             >
2ØØØ             >OUTH   EQU    $2ØØØ   ARBITRARY: 12ØØ BAUD SOFTWARE MOD OF
1EC3             >*                       MIKBUG OUTEEE AS IN LISTING 1.
1EC3             >
1EA3             >       ORG    $1EA3
1EA3 A6 ØØ       >PUN    LDAA   Ø,X      RECORD CHAR. AT X POINTER
1EA5 BD 2Ø ØØ    >       JSR    OUTH        USING HIGH SPEED MOD OF OUTEEE
1EA8 EB ØØ       >       ADDB   Ø,X      ADD LAST SENT CHAR. TO CHECKSUM
1EAA A6 ØØ       >       LDAA   Ø,X      RELOAD A REG. WITH LAST CHAR.
1EAC 81 14       >       CMPA   #$14     IS IT A TURN OFF SIG?
1EAE 27 ØØ       >       BEQ    DEL       YES, GOTO DELAY
1EBØ 81 94       >       CMPA   #$94     IS IT A DIFFERENT TURN OFF SIG?
1EB2             >*                       ( USER SHOULD INSERT HIS OWN TURN OFF
1EB2             >*                         COMMANDS HERE.)
1EB2 27 ØØ       >       BEQ    DEL       YES, GOTO DELAY
1EB4 39          >       RTS              NO, RETURN.
1EB5 37          >DEL    PSHB            SAVE CHECKSUM
1EAF Ø5
1EB3 Ø1
1EB6 C6 ØA       >       LDAB   #$A      SET UP DELAY
1EB8 86 FF       >DE1    LDAA   #$FF
1EBA 4A          >DE2    DECA            DECREMENT A
1EBB 26 FD       >       BNE    DE2      A=Ø? IF NOT, DECREMENT AGAIN
1EBD 5A          >       DECB               IF A=Ø THEN DECREMENT B.
1EBE 26 F8       >       BNE    DE1      B=Ø? IF NOT, CYCLE THRU $FF IN A AGAIN.
1ECØ 33          >       PULB            RESTORE CHECKSUM IN B REG.
1EC1 2Ø DØ       >       BRA    PNON     DELAY OVER, SEND TURN ON SIG.
1EC3             >       END

<<< SYMBOLS >>>


DE1  1EB8  DE2  1EBA  DEL  1EB5  OUTH 2ØØØ  PNON 1E93
PUN  1EA3  C
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MEANWHILE, IC6 IS RUNNING AT 4 X 48ØØ HZ, OR 19,2ØØ HZ. IC3D AND IC3C USE THE RECLOCKED DATA TO SUPPLY CLOCKS TO THE SINEWAVE SYNTHESIZER, IC7, AT EITHER 19.2 KHZ OR 9.6 KHZ, AS DESCRIBED BY LANCASTER. NOTE THAT THE RESISTORS CONNECTED TO THE QØ,Q1,AND Q2 OUTPUTS DIFFER FROM THOSE SHOWN BY LANCASTER. THESE VALUES ARE CORRECT AND ASSURE CANCELLATION OF HARMONICS THROUGH THE 5TH, AS LANCASTER INTENDED.

IC7 IS A 4Ø35, WHICH WAS EASIER FOR ME TO OBTAIN THAN THE 4Ø18 USED BY LANCASTER. IC3A AND IC3B FORCE THE SHIFTING PATTERN TO THE DESIRED GROUP OF FOUR SEQUENTIAL 1'S; THIS LOGIC IS NOT NEEDED WITH THE 4Ø18, AS IT IS INTERNALLY CONNECTED TO PRODUCE ONLY THE DESIRED PATTERN. A SIMPLE RC LOW PASS FILTER SUFFICES TO CLEAN UP THE WAVEFORM AND SUPPRESSES POTENTIAL AUDIO BEATS BETWEEN THE TAPE RECORDER'S BIAS FREQUENCY AND HIGH HARMONICS OF 12ØØ HZ. THE DIVIDER R2,R3 CAN BE SELECTED TO PRESENT ANY DESIRED INPUT LEVEL TO THE TAPE RECORDER.

ON PLAYBACK, THE TAPE RECORDER LOUDSPEAKER TERMINALS ARE CONNECTED TO T-OUT AND T-GND. THESE ARE LOADED BY A 15 OHM, 1 WATT RESISTOR. I RECOMMEND SUCH A LOADING RESISTOR APPROXIMATING THE APPROPRIATE VALUE, RATHER THAN THE USUAL "OPEN CIRCUIT" LOAD USUALLY SEEN IN CASSETTE INTERFACES. THE TAPE RECORDER FREQUENCY RESPONSE WILL USUALLY BE MUCH FLATTER WITH SUCH A LOAD, BECAUSE THE OUTPUT TRANSFORMER SHUNT INDUCTANCE OTHERWISE PROVIDES THE LOAD, WHICH RISES WITH FREQUENCY, AND PRODUCES A DIFFERENTIATED, HIGHLY DISTORED WAVEFORM. SOME RECORDERS HAVE ENOUGH NEGATIVE FEEDBACK TO KEEP THE FREQUENCY RESPONSE FLAT WITH THE LOAD REMOVED, BUT OTHERS MAY ACTUALLY BE UNSTABLE IN THE OPEN-CIRCUIT CONDITION. OF MY TWO RECORDERS, ONE IS UNSTABLE AND THE OTHER STABLE AND INDEPENDENT OF LOAD. ANYHOW, WHILE THE LOAD MAY REDUCE THE PEAK OUTPUT VOLTAGE, IT IS STRONGLY RECOMMENDED, BOTH FOR STABILITY AND WAVEFORM CONTROL. A VALUE TWO TO THREE TIMES THE DESIGN LOAD (SEE TAPE RECORDER INSTRUCTIONS) WILL USUALLY BE A GOOD COMPROMISE BETWEEN OUTPUT LEVEL AND WAVEFORM FIDELITY.

IC9 IS A DUAL 741 OP AMP, ONE SECTION OF WHICH IS USED IN AN ACTIVE BANDPASS FILTER (SEE BELOW), SO I'VE USED THE OTHER SECTION AS A COMPARATOR. THE DIODES CONSTRAIN THE OUTPUT TO SWING FROM Ø TO +5, WHILE THE 1 MEG RESISTOR TO +5 FORCES THE OUTPUT TO Ø IN THE ABSENCE OF SIGNAL.
DECODING THE K.C. WAVEFORM, OR PHASE ENCODING, IS ACCOMPLISHED USING A DUAL MONOSTABLE, IC1, A TYPE 4528. DIODES D5 AND D6 FEED DIFFERENTIATED EDGES OF THE COMPARATOR OUTPUT TO THE DIRECT AND INVERTED TRIGGER INPUTS, TO GENERATE A STRETCHED PULSE FOR EACH ZERO CROSSING. THE DIFFERENTIATED Q OUTPUTS ARE FED TO THE ACTIVE LOW CLEAR DIRECT INPUTS, WHICH RESETS THE MONOSTABLE TIMING CIRCUITS, SO THE DELAY PRODUCED IS INDEPENDENT OF THE TIME BETWEEN TRIGGERS. MS1 PRODUCES A STRETCHED OUTPUT CORRESPONDING TO A HALF CYCLE OF 48ØØ HZ, THUS WHEN THE DATA IS A 1, AND THE TAPE FREQUENCY 24ØØ HZ, MS1'S OUT-

PUT IS A 4800 HZ SQUARE WAVE. THE TRAILING EDGE OF EACH OUTPUT OF MS1 GENERATES A CLOCK PULSE FOR THE DATA RECOVERY FLIPFLOP, IC2A, CLOCKING IT AT THE MIDDLE OF THE NEXT MS1 OUTPUT WHEN THE TAPE FREQUENCY IS 2400, BUT AT THE MIDDLE OF A "MISSING" PULSE WHEN THE TAPE FREQUENCY IS 1200. THIS DECISION IS MADE WITH THE SAME DELAY AFTER A TRANSITION FROM A 1 TO A 0 AS AFTER A TRANSITION IN THE REVERSE DIRECTION, A PROVISION THAT IS IMPORTANT AT 1200 BAUD.

MEANWHILE, THE BANDPASS FILTER EMPLOYING IC9B IS SELECTING THE 4800 HZ COMPONENT OF THE OUTPUT OF MS1. WITH 2400 HZ ON THE TAPE, THE 4800 HZ COMPONENT IS STRONG; WITH 1200 ON THE TAPE, THE FUNDAMENTAL FREQUENCY OF MS1 IS 2400 HZ AND IF THE WAVEFORM WERE A SQUAREWAVE, THE SECOND HARMONIC WOULD BE ABSENT. HOWEVER, THE WAVEFORM IS NOT SQUARE, AND THE 4800 HZ COMPONENT IS STILL STRONG ENOUGH TO BE USED. THE BANDPASS FILTER OUTPUT IS THE SIGNAL OR SYNCH INPUT TO THE PHASE LOCK LOOP. NOTE THAT, SHOULD A PULSE BE MISSING HERE, THE BANDPASS FILTER AND THE PHASE LOCKED LOOP BOTH COMBINE TO KEEP THE CLOCK PULSES SMOOTHLY RUNNING TO THE COMPUTER. IT IS POSSIBLE THE BANDPASS FILTER COULD BE ELIMINATED, BUT WITH IT THE PROBABILITY OF LOCKING ONTO THE CORRECT HARMONIC IS ASSURED. THIS COULD BE A PROBLEM AT 1200 HZ INPUT, AS 2400, 4800, 7200, ETC ARE ALL PRESENT IN MS1'S OUTPUT.

THE RS232 LINE IS DRIVEN BY Q2, WHOSE COLLECTOR IS TIED TO GROUND THROUGH R7. TRUE RS232 LINE SPECS WOULD REQUIRE RETURNING R7 TO -12, BUT IN MY CASE, THE LINE IS ALREADY PULLED DOWN TO - 12 BY THE COMPUTER OR TERMINAL, AND R7 IS USED ONLY TO DEFINE THE COLLECTOR VOLTAGE OF Q2 WHEN THE LINES ARE DISCONNECTED.

IC10 SUPPLIES -5 VOLTS TO THE 741 OP AMPS AND THE LM565 PLL.

IC4A AND IC4B COMPRISE A FLIP-FLOP TO CONTROL THE TAPE RECORDER MOTOR USING PULSES COUPLED FROM THE CT1024 CURSOR CONTROL DECODER CIRCUITS. S3 OVERRIDES THESE PULSES IN ITS "OFF" AND "ON" POSITIONS. Q3 AND Q4 ARE ARRANGED TO SIMULATE A MOTOR CONTROL SWITCH CONNECTED BETWEEN B+ OF THE TAPE RECORDER AND A MOTOR THAT IS RETURNED TO GROUND. THIS CAN BE REARRANGED TO SUIT OTHER TAPE RECORDER SETUPS. Q4 IS A SILICON POWER TRANSISTOR OF THE UNNUMBERED RADIOSHACK VARIETY. A 30 VOLT, 0.5 AMP COMBINATION SHOULD BE SUITABLE. POWER RATING IS NOT IMPORTANT; THE SATURATED COLLECTOR-EMITTER DROP SHOULD NOT EXCEED ABOUT 0.3 VOLTS, CORRESPONDING TO LESS THAN ONE WATT DISSIPATION.

IC4D COMBINES DATA ABSENT AND MOTOR CONTROL SIGNALS TO "RELEASE" THE RS232 LINE WHEN THE INTERFACE IS NOT SENDING OUTPUT DATA ON IT. THE COMPARATOR OUTPUT IS DETECTED BY DIODE D7 TO CONTROL IC4C, WHICH SELECTS EITHER THE CLOCK SIGNAL COMING FROM THE TAPE, OR THE CLOCK OUTPUT FROM THE COMPUTER WHEN TAPE DATA IS ABSENT. THE MASTER RESET OF THE SINEWAVE SYNTHESIZER IS ALSO CONTROLLED BY THE DATA PRESENT SIGNAL TO SUPPRESS SYNTHESIZER

ACTION AND TAPE RECORDER INPUT DURING PLAYBACK.

WELL, THAT'S THE STORY OF MY "CONQUERING" OF THE 1200 BAUD MT EVEREST. I'VE USED SWTP'S SERIAL CONTROL INTERFACE WITHOUT HARDWARE MODIFICATION, PROVIDED SINEWAVE RECORDING AND A VERY STABLE CLOCK RECOVERY CIRCUIT, AND DONE IT ALL WITH SOFTWARE MODIFICATIONS. ONLY ONE SWITCH IS NEEDED TO CHANGE BAUD RATE AND IT IS CONVENIENTLY LOCATED AT THE CASETTE RECORDER INTERFACE. I FIND THAT I CAN CHANGE TAPE RECORDER VOLUME AND TONE SETTINGS OVER WIDE RANGES WITHOUT AFFECTING PERFORMANCE - WHICH MEANS RELIABILITY. I CAN USE RATHER POOR QUALITY TAPES WITH -20 DB (X 1/10 AMPLITUDE) DROPOUTS, ALTHOUGH SUCH IS ALWAYS RISKY.

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